μPD72105
OMNINET LOCAL AREA NETWORK CONTROLLER

PRELIMINARY INFORMATION

Description

The μPD72105 provides local area network (LAN) communications implementing the OMNINET® I and II protocols in a single CMOS 48-pin DIP. The device can transmit data at a rate of up to 4 Mb/s using RS-422 bus transmitters and receivers. The controller responds to 17 OMNINET commands using the on-chip CPU.

The chip also contains a DMA controller with four independent channels for use with an 8- or 16-bit data bus, and can address a 16M-byte address space. The transmit section contains a 12-byte FIFO and the receiver contains a 20-byte FIFO to accommodate the high data rate. The OMNINET controller provides network diagnostics capability as well as CRC generation and checking using a 16- or 32-bit CRC for data reliability.

The μPD72105 provides a single chip solution to LAN implementation. The excellent memory addressing and data handling capability of this controller can significantly reduce the overhead on the system CPU.

OMNINET is a registered trademark of Corvus Systems.

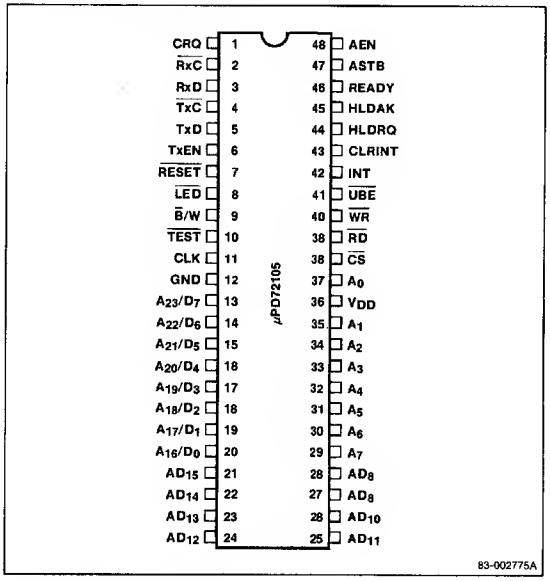
Features

- ☐ Fully implements OMNINET I and II protocols
- ☐ Data rates up to 4 Mbps
- ☐ 17 OMNINET commands
- ☐ On-chip CPU
- ☐ On-chip DMAC with four independent channels
- ☐ 8- or 16-bit data bus
- ☐ 16M-byte (2^{24}) address space for dual-ported local or global memory
- ☐ 12-byte transmitter FIFO
- ☐ 20-byte receiver FIFO
- ☐ 16- or 32-bit CRC
- ☐ On-chip 40-MHz DPLL
- ☐ Network diagnostics
- ☐ 8-MHz system clock input, independent of serial clock
- ☐ CMOS technology

Ordering Information

Part No.	Package Type
μPD72105C	48-pin plastic DIP
μPD72105L	52-pin PLCC (Available 4Q86)

Pin Configuration



Pin Identification

No.	Symbol	Function
1	CRQ	Command request input
2	$\overline{RxC}$	Receive clock input
3	RxD	Receive data input
4	$\overline{TxC}$	Transmit clock input/output
5	TxD	Transmit data output
6	TxEN	Transmit enable output
7	$\overline{RESET}$	System reset from host computer
8	$\overline{LED}$	LED drive output, general purpose output
9	$\overline{B}/W$	Byte/word mode select input
10	$\overline{TEST}$	Test input, must be held high for normal operation
11	CLK	System clock input
12	GND	System ground
13-20	A_{23}/D_7 to A_{16}/D_0	Multiplexed address bits 16-23 and data bus bits 0-7. These signals are bidirectional.
21-28	AD_{15}/AD_8	Multiplexed address bits 8-15 and data bus bits 8-15. These signals are bidirectional.
29-35	A_7-A_1	Address bits 1 to 7; bit 1 is an input/output, bits 2-7 are output only.

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Pin Identification (cont)

No.	Symbol	Function
36	V_{DD}	+5 V (typical)
37	A_0	Address bit 0, input/output
38	$\overline{CS}$	Chip select input from host computer; input
39	$\overline{RD}$	Read control signal from host computer; input
40	$\overline{WR}$	Write control signal from host computer; input
41	$\overline{UBE}$	Upper byte enable input/output
42	INT	Interrupt request output
43	CLRINT	Clear interrupt request input
44	HLDRQ	Hold request output
45	HLDAK	Hold acknowledge input
46	READY	Ready input
47	ASTB	Address strobe output
48	AEN	Address enable output

Block Diagram